CLAIMS

1. A differential oscillator comprising:

a first transistor having first and second end terminals and a first control terminal;

a second transistor having third and fourth end terminals and a second control terminal;

means for coupling the first control terminal to one of the end terminals of the second transistor and the second control terminal to the corresponding end terminal of the first transistor;

means for biasing the first and second transistors to oscillate;

a differential output formed between corresponding end terminals of the first and second transistors; and

a reference crystal connected across the differential output to establish the frequency across the differential output.

2. The differential oscillator of claim 1, in which the oscillator is part of an integrated circuit chip, the differential output of the oscillator is coupled to external terminals on the chip, the crystal is disposed off the chip, and the crystal is connected to the external terminals.

3. The differential oscillator of claim 1, in which the coupling means comprises a first RC timing circuit connected between the first control terminal and the one end terminal of the second transistor and a second RC timing circuit connected between the second control terminal and the one end terminal of the first transistor, the RC timing circuits determining the natural frequency at which the oscillator oscillates in the absence of the crystal reference.

4. The differential oscillator of claim 1, additionally comprising a buffer amplifier having a differential input connected across the differential output.

5. The differential oscillator of claim 1, in which the crystal reference is a quartz crystal.

6. A crystal oscillator including:

a resonator circuit, defining a symmetrical pair of output terminals;

an active oscillator circuit, coupled to the resonator circuit output terminals, thus creating differential sinusoidal signals of substantially the same amplitude at the symmetrical pair of resonator circuit output terminals; and

a linear buffer amplifier, coupled to receive the differential sinusoidal signals thus created by the resonator circuit and active oscillator circuit interaction, and providing a differential sinusoidal output signal at a pair of output terminals.

7. A crystal oscillator including:

a linear buffer amplifier, coupled to receive the differential sinusoidal signals, and providing a differential sinusoidal output signal at a pair of output terminals; and

a non linear buffer amplifier, cascaded after the linear buffer amplifier such that the differential sinusoidal signal are transformed into a differential periodic reference signal in operative response to the differential sinusoidal input.

8. A crystal oscillator including:

a resonator circuit, defining a symmetrical pair of output terminals;

an active oscillator circuit, coupled to the resonator circuit output terminals, and thus creating differential sinusoidal signals at the symmetrical pair of output terminals;

a linear buffer amplifier, coupled to receive the differential sinusoidal signals thus created by the resonator circuit and active oscillator circuit interaction, and providing a differential sinusoidal output signal at a pair of output terminals; and

a non linear buffer amplifier, cascaded after the linear buffer amplifier such that the differential sinusoidal signal is transformed into a differential periodic reference signal in operative response to the differential sinusoidal input.

9. The crystal oscillator circuit of claim 8 wherein the resonator circuit comprises:

a crystal;

a first capacitor shunted to ground from a first terminal of the crystal; and

a second capacitor shunted to ground from a second terminal of the crystal.

10. The crystal oscillator circuit of claim 8 wherein the active oscillator circuit further comprises a differential pair of transistors implemented such that feed back in the circuit limits transistor gain thus preventing latch up of the active oscillator circuit output at frequencies above the cut off frequencies of the high pass filters.

11. The crystal oscillator circuit of claim 8 in which the active oscillator circuit comprises high pass filters in the path of each resonator lead such that low frequencies are rejected thereby preventing latch up of the crystal oscillator circuit output at frequencies below the cut off frequencies of the filters.

12. The crystal oscillator circuit of claim 8 wherein the active oscillator circuit further comprises a gain device, providing positive feed back to the resonator.

13. The crystal oscillator circuit of claim 8 in which the active oscillator stage comprises:

a first high pass filter in the path of the first resonator terminal; and

a second high pass filter in the path of the second resonator terminal;

whereby low frequencies are rejected, preventing latch up of the circuit output at frequencies below the cut off frequencies of the filters.

14. The crystal oscillator circuit of claim 8 in which the linear buffer amplifier comprises:

means for presenting a high impedance at the input thereby preventing resonator loading; and

bias means for operating the linear buffer amplifier in the bias region producing linear amplification.

15. The crystal oscillator circuit of claim 8 in which the linear buffer amplifier comprises means for producing substantially unity signal gain.

16. The crystal oscillator circuit of claim 8 in which the linear buffer amplifier comprises means for producing signal gain substantially within the range of 0.95 to 1.05.

17. The crystal oscillator circuit of claim 8 wherein the nonlinear buffer amplifier comprises means for transforming a sine wave input to a square wave output, whereby output jitter is reduced to produce a stable reference clock.

18. The crystal oscillator of claim 8 in which the nonlinear buffer amplifier comprises amplification means to transform a sine wave input to CML square wave output.

19. A crystal oscillator circuit comprising:

a crystal resonator having differential outputs;

an active oscillator circuit having differential outputs cascaded with the crystal resonator such that the differential outputs produced by the circuit interactions are sinusoidal signals;

a linear buffer amplifier having differential inputs coupled to the point where the cascaded resonator and active oscillator circuit are connected, and thus providing a differential output without degrading the resonator and active circuit interaction; and

at least one nonlinear buffer amplifier having differential inputs coupled to the differential outputs of the linear buffer amplifier and producing a differential output signal.

20. The crystal oscillator of claim 19 further comprising a non linear buffer amplifiers coupled to the linear buffer amplifier output.

21. A crystal oscillator circuit comprising:

a differential active network having differential output terminals;

a differential linear buffer amplifier having a differential input and output terminals;

a resonator coupled across the terminals of the differential active network and the input to the buffer amplifier; and

at least one differential nonlinear buffer amplifier coupled to the output terminals of the linear buffer amplifier for producing one or more differential output signals.

22. The crystal oscillator circuit of claim 21 in which the resonator includes:

a crystal;

a first capacitor shunted to ground from the first terminal of the crystal; and

a second capacitor shunted to ground from the second terminal of the crystal.

23. The crystal oscillator circuit of claim 21 in which the differential active oscillator circuit includes high pass filters in the path of each resonator lead such that low frequencies are rejected in order to prevent latch up of the circuit output at frequencies below the cut off frequencies of the filters.

24. The crystal oscillator of claim 21 in which the differential active oscillator circuit additionally includes a differential pair of transistors implemented such that feed back in the circuit limits transistor gain, thus preventing latch up of the circuit output at frequencies above the cut off frequencies of the high pass filters.

25. The crystal oscillator of claim 21 in which the differential linear buffer amplifier comprises:

means to present a high input impedance to prevent resonator loading; and

bias means to operate the differential buffer amplifier in the operating region of linear amplification.

26. The crystal oscillator of claim 21 in which the differential nonlinear buffer amplifier comprises amplification means to transform a sine wave input to a square wave output.

27. The crystal oscillator of claim 21 in which the nonlinear buffer amplifier comprises amplification means to transform a sine wave input to CML square wave output.

28. A method for generating a stable differential clock signal comprising the steps of:

generating a differential sinusoidal signal across the terminals of a crystal;

high pass filtering the signal present at each terminal of the crystal;

amplifying each signal that has been high pass filtered with reduced gain as signal amplitude increases;

buffering the differential signal that is present at across the terminals of the crystal;

linearly amplifying the buffered signal; and

nonlinearly amplifying the previously linearly amplified buffer signal.

29. The method of claim 28 in which the step of nonlinear amplification produces an essentially square wave output.

30. A method for generating a stable differential clock signal comprising the steps of:

generating a differential sinusoidal signal across the terminals of a crystal;

linearly amplifying the differential signal; and

nonlinearly amplifying the linearly amplified signal, while maintaining a differential signal throughout and producing a differential output signal.

31. A crystal oscillator comprising:

a one port resonator having two terminals to facilitate the establishment of a differential sinusoidal signal between the terminals, that is coupled to;

a one port active oscillator circuit having two terminals that are coupled to the one port resonator terminals whereby, the resulting signal produced at the coupled terminals is a differential sinusoidal signal characterized by substantially equal amplitudes, and a phase difference of substantially one hundred and eighty degrees;

a first capacitor shunted to ground from the first terminal of the one port resonator;

a second capacitor shunted to ground from the second terminal of the one port resonator;

a two port buffer amplifier providing a high impedance differential input port and an output port, with each port consisting of two terminals, having its input port coupled to the coupling established between the one port resonator and one port active oscillator circuit such that the differential signal present is not perturbed, and having its output port coupled to; and

a two port nonlinear amplifier having differential inputs and outputs, with each port consisting of 2 terminals, with its input port coupled to the output of the two port buffer

amplifier wherein the input is a differential sinusoid and the output produced is a differential square wave of the same frequency as the input, characterized by substantially equal amplitudes, and a phase difference of substantially one hundred and eighty degrees.

32. The crystal oscillator of claim 31 wherein additional non linear buffer amplifiers inputs are coupled to the linear buffer amplifier's output wherein the input is a differential sinusoid and the outputs produced are differential square waves of the same frequency as the input, with each non linear amplifier's output characterized by substantially equal amplitudes, and a phase difference of substantially one hundred and eighty degrees between the pins.

33. The crystal oscillator of claim 31, wherein the differential square wave amplitudes at the output ports of the additional non linear buffers are set to various differing logic levels.

34. A phase locked loop comprising:

reference oscillator means for generating a low phase noise reference frequency;

a voltage controlled oscillator (VCO) for producing a desired output frequency;

a phase detector for comparing the phase of the reference signal to the divided down VCO signal; and

a loop filter for suppressing reference frequency components and integrating.

35. The phase locked loop of claim 34, further comprising a programmable divider for dividing down the VCO signal.

36. A frequency synthesizer comprising:

an oscillator means for generating a stable differential reference signal;

a divide by integer counter for dividing the frequency generated in the oscillator down to a known lower value;

a voltage controlled oscillator for generating a desired output frequency in response to an applied substantially DC voltage;

a divide by integer counter for dividing the output frequency down to a known lesser value;

a phase detector for comparing the divided down reference frequency to the divided down output frequency, whereby an error voltage proportional to the difference in phase and frequency is produced; and

a low pass filter for converting the error voltage to a DC error voltage.

37. A CATV tuner comprising:

a substrate upon which a substantial portion of the tuner circuitry is disposed, and having an RF input connection and an intermediate frequency output connection;

a reference oscillator means for providing a stable low noise, differential clock signal;

a phase locked loop using the differential low noise reference oscillator signal as a frequency reference to produce a local oscillator signal;

a filter to selectively remove spurious frequency components created in the tuner or received from an external source, and undesired to be present at the output of the tuner; and

a mixer that utilizes a local oscillator signal to produce an intermediate frequency that is more easily processed by subsequent circuitry.

38. A television set top box comprising:

a transceiver for receiving programming and ordering services;

an oscillator means to provide a reference frequency that is used in the frequency conversion of a received signal;

a decryption circuit allowing premium programming to be received and descrambled such that it is viewable;

a memory to store information; and

a decoder to produce an audio and video signal.

39. A television comprising:

a CATV tuner circuit for reception of incoming television signals at radio frequencies;

an oscillator means to provide a reference signal in the receiver enabling the frequency conversion of the incoming television circuit to be performed;

audio signal processing means for processing the television signal such that it may be heard;

video signal processing means for producing signals that create an image on a display device; and

a display device that is capable of reproducing an image that is contained in the transmitted incoming television signal.

40. A VCR comprising:

a CATV tuner circuit for reception of incoming television signals at radio frequencies;

an oscillator means to provide a reference signal in the receiver enabling the frequency conversion of the incoming television circuit to be performed;

audio signal processing means for processing the television signal such that it may be heard;

video signal processing means for producing signals that create an image on a display device;

a memory for storing a instructions;

a recording and play back unit that allows the VCR to play and record information stored on a recording media; and

a signal switching unit for connecting the recording and playback unit in and out of the signal path.

41. A cable modem comprising:

a CATV tuner circuit for reception of incoming television signals at radio frequencies;

an oscillator means to provide a reference signal in the receiver enabling the frequency conversion of the incoming television circuit to be performed;

an Ethernet transceiver for connecting the cable television network to the Ethernet;

a diplexer that allows full duplex communication over the CATV network.

a modulator for encoding data for upstream transmission; and

a demodulator for decoding downstream data received.